**Assignment:** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

Copy-paste or type the unique URL of your assignment solution from website [www.edaplayground.com](http://www.edaplayground.com) for assignment questions. Please note that do not copy someone else’s link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

1. Write the single Verilog code and testbench for 3-input gates (AND, OR, NAND, NOR, EXOR, EXNOR) using gate level modeling.

**Ans: Link1:** [**https://www.edaplayground.com/x/7uFp**](https://www.edaplayground.com/x/7uFp)

1. Write the Verilog code and testbench for 3-input gates (AND, OR) using structural modeling use two 2-input gates.

**Ans: Link2:** [**https://www.edaplayground.com/x/eAhg**](https://www.edaplayground.com/x/eAhg)

1. Verilog code and testbench for finding 1’s complement of 8-bit binary number.

**Ans: Link3:** [**https://www.edaplayground.com/x/LHwW**](https://www.edaplayground.com/x/LHwW)